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L1 and (adapter adj1 card)	1

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DB=USPT; PLUR=YES; OP=OR			
L4	L1 and (adapter adj1 card)	1	L4
L3	L1 same adapter	0	L3
L2	L1 same (adapter adj1 card)	0	L2
L1	(board or card) same bus same socket same configur$5 same indicat$3	43	L1

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Search Results -

Terms	Documents
L1 and (adapter adj1 card)	0

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Search: L5

Refine Search

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Search History

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DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L1 and (adapter adj1 card)	0	L5
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and (adapter adj1 card)	1	L4
L3	L1 same adapter	0	L3
L2	L1 same (adapter adj1 card)	0	L2
L1	(board or card) same bus same socket same configur$5 same indicat$3	43	L1

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(board or card) and bus and config* and (socket or c Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **FDTD and experimental investigation of EMI from stacked-card PCB configurations**
Hockanson, D.M.; Xiaoning Ye; Drewniak, J.L.; Hubing, T.H.; Van Doren, T.P. Dubroff, R.E.;
Electromagnetic Compatibility, IEEE Transactions on , Volume: 43 , Issue: 1 , 2001
Pages:1 - 10

[Abstract] [PDF Full-Text (396 KB)] **IEEE JNL**

---

2 **A new distributed real-time controller for robotics applications**
Buhler, M.; Whitcomb, L.; Levin, F.; Koditschek, D.E.;
COMPCON Spring '89. Thirty-Fourth IEEE Computer Society International Conference: Intellectual Leverage, Digest of Papers. , 27 Feb.-3 March 1989
Pages:63 - 69

[Abstract] [PDF Full-Text (652 KB)] **IEEE CNF**

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3 **An implementation of IEEE 1451 NCAP for Internet access of serial based sensors**
Wobschall, D.;
Sensors for Industry Conference, 2002. 2nd ISA/IEEE , 19-21 Nov. 2002
Pages:157 - 160

[Abstract] [PDF Full-Text (350 KB)] **IEEE CNF**

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4 **PC/104-ISA t PCI**
Brown, M.F.;
WESCON/98 , 15-17 Sept. 1998
Pages:210 - 215

[Abstract] [PDF Full-Text (776 KB)] **IEEE CNF**

5 **A real time visi n architecture using a dynamically rec nfigurable f bus**

Al-Awa, M.N.; Fristot, V.; Coulon, P.Y.; Charras, J.P.; Chehikian, A.;

Image Processing and its Applications, 1995., Fifth International Conference c
6 Jul 1995
Pages:470 - 474

[Abstract] [PDF Full-Text (348 KB)] **IEE CNF**

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FDTD and experimental investigation of EMI from s card PCB configurations

Hockanson, D.M. Xiaoning Ye Drewniak, J.L. Hubing, T.H. Van Doren, T.P. Dubrc
Missouri Univ., Rolla, MO, USA;

This paper appears in: **Electromagnetic Compatibility, IEEE Transacti ns**

Publication Date: Feb. 2001
On page(s): 1 - 10
Volume: 43 , Issue: 1
ISSN: 0018-9375
Reference Cited: 15
CODEN: IEMCAE
Inspec Accession Number: 6908048

Abstract:
Stacked-**card** and modules-on-backplane printed circuit-**board** geometries ar advantageous for conserving real-estate in many designs. Unfortunately, at h frequencies, electromagnetic magnetic interference (EMI) resulting from the nonnegligible impedance of the signal return at the **connector** may occur. Th EMI coupling path results in the daughtercard being driven against the mothe attached cables, resulting in common-mode radiation. The **connector** geome modified to minimize the EMI coupling path when high frequencies are routed the motherboard and daughtercard. Current speeds and printed circuit **board** result in geometries that are of significant dimensions in terms of a waveleng upper frequency end of the signal spectrum. The PCB geometries are then of electrical extent to be effective EMI antennas. The resonant lengths of the EM may, however, be quite removed from the typical half-wavelength dipole resc The finite difference time-domain method can be used to numerically analyze circuit **board** geometries, determine antenna resonances, and investigate EM paths. EMI resulting from the stacked-**card configuration** has been investig experimentally and numerically to ascertain the EMI coupling path at the **bus connector**, and EMI antennas

Index Terms:
antennas electric **connectors** electromagnetic coupling electromagnetic interference difference time-domain analysis printed circuits resonance system buses EMI EM EMI coupling path FDTD PCB size antenna resonances **bus connector** cables

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mode radiation **connector** geometry daughtercard electromagnetic magnetic interfe difference time-domain method high frequencies modules-on-backplane motherboar circuit-**board** geometries resonant lengths signal return signal spectrum stacked-ca **configurations** wavelength

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Documents that cite this document
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Reference list:

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[Abstract] [PDF Full-Text (916KB)]

2, J. R. Bergervoet, "EMC measurements and models connecting the system the module level," *Phillips J. Res.*, vol. 48, pp. 63-80, 1994.
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3, F. B. M.van Horck, *Electromagnetic Compatibility and Printed Circuit Boarc* Eindhoven, The Netherlands: Tech. Univ. Eindhoven, 1998.
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4, A. E. Ruehli, "Inductance calculations in a complex integrated circuit envir *IBM J. Res. Develop.*, vol. 16, pp. 470-481, 1972.
[Buy Via Ask*IEEE]

5, K. Li, M. A. Tassoudji, S. Y.Poh, M.Tsuk, R. T.Shin, and J. A.Kong, "FD-TD electromagnetic radiation from modules-on-backplane configurations," *IEEE T Electromagn. Compat.*, vol. 37, pp. 326-332, Aug. 1995.
[Abstract] [PDF Full-Text (632KB)]

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[Abstract] [PDF Full-Text (396KB)]

7, D. M.Pozar, *Microwave Engineering* Reading, MA: Addison-Wesley, 1990.
[Buy Via Ask*IEEE]

8, A.Taflove, *Computational Electrodynamics: The Finite-Difference Time-Doı Method* Boston, MA: Artech House, 1995.
[Buy Via Ask*IEEE]

9, K. S.Kunz and R. J.Luebbers, *The Finite Difference Time Domain, Method f Electromagnetics* Boca Raton, FL: CRC Press, 1993.
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10, K. R. Umashankar, A.Taflove, and B.Beker, "Calculation and experimenta of induced currents on coupled wires in an arbitrary shaped cavity," *IEEE Trar Antennas Propagat.*, vol. 35, pp. 1248-1257, Nov. 1987.
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[Abstract] [PDF Full-Text (828KB)]

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[Abstract] [PDF Full-Text (1228KB)]

13, P. Berenger, "A perfectly matched layer for the absorption of electromagı waves," *J. Comput. Phys.*, vol. 114, no. 2, pp. 185-200, 1994.
[CrossRef] [Buy Via Ask*IEEE]

14, W.Stutzman and G.Thiele, *Antenna Theory and Design* New York: Wiley,
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15, C. R.Paul, *Introduction to Electromagnetic Compatibility* New York: Wiley
[Buy Via Ask*IEEE]

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A real time vision architecture using a dynamically reconfigurable fast bus

Al-Awa, M.N. Fristot, V. Coulon, P.Y. Charras, J.P. Chehikian, A.
LTIRF-INPG

This paper appears in: **Image Processing and its Applications, 1995., Fif International Conference on**

Meeting Date: 07/04/1995 - 07/06/1995
Publication Date: 4-6 Jul 1995
Location: Edinburgh UK
On page(s): 470 - 474
Reference Cited: 20
Inspec Accession Number: 5028457

Abstract:
Different existing vision machines are surveyed. The authors are particularly i their intercommunication system, which is a fundamental factor in the overall performance. In order to fulfil the need for a flexible, high-performance, and effective vision machine a coarse-grain architecture is proposed. It is based o dynamically reconfigurable fast **bus**. The authors are developing a prototype This prototype, hosted by a PC, uses a VME-like back plane cabinet in which t **connector** is used for the **configuration** control lines and the P2 **connector** implementation of 4 fast transfer lines channels. The DRIFT interface is desig achieve a bandwidth of 1 Gbits/s. Processing modules are built on extended d Eurocards on which the DRIFT interface occupies 25% of the whole **board** su prototype will be used in some vision applications in which broadcasting and reconfiguration are necessary

Index Terms:
CCL DRIFT interface FTL channels Fastbus P1 **connector** P2 **connector** VME-plane cabinet bandwidth broadcasting coarse-grain architecture computer vision processing chips dynamically reconfigurable fast **bus** extended double Eurocards im processing equipment intercommunication system parallel architectures prototype m time vision architecture real-time systems reconfigurable architectures vision machin DRIFT interface FTL channels Fastbus P1 **connector** P2 **connector** VME-like ba cabinet bandwidth broadcasting coarse-grain architecture computer vision digital processing chips dynamically reconfigurable fast **bus** extended double Eurocards im processing equipment intercommunication system parallel architectures prototype m time vision architecture real-time systems reconfigurable architectures vision machin

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☐ 1. Document ID: US 6564274 B1

L3: Entry 1 of 13 File: USPT May 13, 2003

US-PAT-NO: 6564274
DOCUMENT-IDENTIFIER: US 6564274 B1

TITLE: Modular architecture for small computer networks

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6421754 B1

L3: Entry 2 of 13 File: USPT Jul 16, 2002

US-PAT-NO: 6421754
DOCUMENT-IDENTIFIER: US 6421754 B1

TITLE: System management mode circuits, systems and methods

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 5872983 A

L3: Entry 3 of 13 File: USPT Feb 16, 1999

US-PAT-NO: 5872983
DOCUMENT-IDENTIFIER: US 5872983 A

TITLE: Power management interface system for use with an electronic wiring board article of manufacture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 5870621 A

L3: Entry 4 of 13 File: USPT Feb 9, 1999

US-PAT-NO: 5870621
DOCUMENT-IDENTIFIER: US 5870621 A

h e b b g e e e f e f ef b e

TITLE: Quadrilateral multichip computer systems and printed circuit boards therefor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 5867717 A

L3: Entry 5 of 13 File: USPT Feb 2, 1999

US-PAT-NO: 5867717
DOCUMENT-IDENTIFIER: US 5867717 A

TITLE: Dynamic system clocking and address decode circuits, methods and systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5864702 A

L3: Entry 6 of 13 File: USPT Jan 26, 1999

US-PAT-NO: 5864702
DOCUMENT-IDENTIFIER: US 5864702 A

TITLE: Computer system power management interconnection circuitry, systems and methods

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5845132 A

L3: Entry 7 of 13 File: USPT Dec 1, 1998

US-PAT-NO: 5845132
DOCUMENT-IDENTIFIER: US 5845132 A

TITLE: Computer system power management interconnection circuitry, system and methods

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 8. Document ID: US 5835733 A

L3: Entry 8 of 13 File: USPT Nov 10, 1998

US-PAT-NO: 5835733
DOCUMENT-IDENTIFIER: US 5835733 A

TITLE: Method and apparatus for implementing a single DMA controller to perform DMA operations for devices on multiple buses in docking stations, notebook and desktop computer system

h e b b g e e e f e f ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 9. Document ID: US 5781780 A

L3: Entry 9 of 13 File: USPT Jul 14, 1998

US-PAT-NO: 5781780
DOCUMENT-IDENTIFIER: US 5781780 A

TITLE: Power management supply interface circuitry, systems and methods

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 5754436 A

L3: Entry 10 of 13 File: USPT May 19, 1998

US-PAT-NO: 5754436
DOCUMENT-IDENTIFIER: US 5754436 A

TITLE: Adaptive power management processes, circuits and systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Terms	Documents
L1 and L2	13

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L3: Entry 12 of 13 File: USPT Mar 3, 1998

US-PAT-NO: 5724529
DOCUMENT-IDENTIFIER: US 5724529 A

TITLE: Computer system with multiple PC card controllers and a method of controlling I/O transfers in the system

DATE-ISSUED: March 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Smith; Stephen A.	Palo Alto	CA		
Naji; Jafar	Glenbare	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Cirrus Logic, Inc.	Fremont	CA			02

APPL-NO: 08/ 561777 [PALM]
DATE FILED: November 22, 1995

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/309; 395/306, 395/281, 395/284, 395/822, 395/829, 395/651
US-CL-CURRENT: 710/1; 710/104, 710/2, 710/9, 713/1

FIELD-OF-SEARCH: 395/500, 395/850, 395/653, 395/829, 395/421, 395/309, 395/205, 395/306, 395/281, 395/284, 395/822, 395/651, 395/200

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4954949	September 1990	Rubin	395/200.01
☐	5038320	August 1991	Heath et al.	395/830
☐	5111423	May 1992	Kopec, Jr. et al.	395/500
☐	5237690	August 1993	Bealkowski et al.	395/653
☐	5274711	December 1993	Hamilton et al.	395/829
☐	5446869	August 1995	Padgett et al.	395/500
	5507002	April 1996	Heil	395/828

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☐				
☐	5530895	June 1996	Enstrom	395/421.02
☐	5555510	September 1996	Verseput et al.	364/514R
☐	5572688	November 1996	Sytwu	395/309
☐	5590377	December 1996	Smith	395/842

ART-UNIT: 237

PRIMARY-EXAMINER: Shin; Christopher B.

ATTY-AGENT-FIRM: Stewart; David L. Violette; J. P.

ABSTRACT:

A method and arrangement for controlling input/output (I/O) operations in a computer system provides multiple PC card controllers but allows legacy software to be used. A PCI bus is coupled to a central processing unit, and an ISA bus is coupled to the PCI bus by a bridge. At least one PC card controller is coupled to the PCI bus and at least one other PC card controller is coupled to the ISA bus. Each PC card controller has at least one socket in which a device is connectable, each socket being separately addressable by the processor at an (I/O) address through the respect PC card controller. Each controller also has a socket pointer register, each socket pointer register being loadable with socket pointer information that uniquely identifies each socket of the controller among all of the sockets of the plurality of controllers in the computer system. Each controller also has an index register and a plurality of data registers, the index stored in the index register pointing to one of the data registers. The index registers of the PC card controllers are updated when the processor writes to an I/O address, without acknowledging the write on the PCI bus. This allows the writes to propagate through the system to lower levels, instead of being stopped by a subtractive decode device. To perform this, each PC card controller compares the socket pointer information with the updated index in the index register. When at least a portion of the socket pointer information matches at least a portion of the updated index, the PC card controller updates with write data the data register pointed to by the index register.

20 Claims, 3 Drawing figures

L1: Entry 3 of 43 File: USPT May 13, 2003

DOCUMENT-IDENTIFIER: US 6564274 B1
TITLE: Modular architecture for small computer networks

Detailed Description Text (13):
The configuration and usage of client cards as personal computers serving remote users (via external connections 19-21 to personal computer accessories) is indicated in FIG. 3. As seen here, client cards 30 and 31 attach removably to a system board 32, via not shown socket structures affixed to the board, and connect to a system bus 33 contained on the same board. Bus 33 preferably is configured and operated in accordance with previously noted published specifications for PCI buses. System board 32 constitutes the principal substrate of the system, and the host computer system and resources managed by it (including disk storage and RAM memory) are mounted directly on that substrate. Connections extend from bus 33 to the client computers, via their not-shown sockets) and to the host system and its resources. These bus connections enable the client cards to exchange data with each other, with the host system, and with resources managed by the host system.

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L1: Entry 3 of 43 File: USPT May 13, 2003

US-PAT-NO: 6564274
DOCUMENT-IDENTIFIER: US 6564274 B1

TITLE: Modular architecture for small computer networks

DATE-ISSUED: May 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heath; Chester A.	Chapel Hill	NC		
McBride; Dennis J.	Wake Forest	NC		
McKnight; Gregg J.	Chapel Hill	NC		
Wu; Vincent C.	Apex	NC		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Omnicluster Technologies, Inc.	Boca Raton	FL			02

APPL-NO: 09/ 466463 [PALM]
DATE FILED: December 17, 1999

PARENT-CASE:
CROSS-REFERENCES TO RELATED APPLICATIONS Application Ser. No. 09/465,675 by R. Callender et al, filed at the same time as the present application and titled PEER NETWORKING IN CONCENTRATED COMPUTER CLUSTERS, describes a computer system conforming to the modular architecture described in the present application which uses network communication protocols on a bus connecting a group of computers housed within a small enclosure/box.

INT-CL: [07] G06 F 13/42

US-CL-ISSUED: 710/105; 710/11, 710/301, 333/236, 333/243, 709/244
US-CL-CURRENT: 710/105; 333/236, 333/243, 709/244, 710/11, 710/301

FIELD-OF-SEARCH: 710/105, 709/219, 709/230, 348/14, 348/15, 348/17, 370/85.6, 380/49, 395/425, 395/474, 333/236, 333/243, 333/245

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

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☐	4639864	January 1987	Katzman et al.	713/340
☐	5067071	November 1991	Schanin et al.	395/275
☐	5239643	August 1993	Blount et al.	395/425
☐	5381413	January 1995	Tobagi et al.	370/85.6
☐	5765036	June 1998	Lim	395/474
☐	5927050	July 1999	Houck et al.	53/428
☐	6011579	June 2000	Newlin	348/15
☐	6075863	June 2000	Krishnan et al.	380/49
☐	6085273	July 2000	Ball et al.	710/129
☐	6289376	September 2001	Taylor et al.	709/219

OTHER PUBLICATIONS

Robert G. winch, Telecommunication Transmission Systems 1993, McGraw-Hill, 1.sup.st edition, p487-p500.

ART-UNIT: 2189

PRIMARY-EXAMINER: Lefkowitz; Sumati

ASSISTANT-EXAMINER: Lee; Christopher E.

ATTY-AGENT-FIRM: Kaplan & Gilman, LLP

ABSTRACT:

In concentrated multiprocessor systems conforming to the presently disclosed modular architecture, a host processor and plural client processors are packaged in a single box containing a high speed (short length) bus connecting all of the processors, and data storage resources via the bus. The bus may be of a type commonly used in contemporary single computer systems; e.g. one conforming to PCI specifications. The host processor and associated resources are mounted directly on an integrated circuit motherboard containing the bus and card connectors attached to the bus. The card connectors removably receive integrated circuit cards containing individual client processors. In one embodiment, client processors are configured to be used as workstations or PC's--in a residence, office or small factory environment--relative to users and accessories remote from the system enclosure. In another embodiment, host and client processors are configured to operate as servers between the system and multiple data networks external to the system; the host and client subsystems thereby constituting a server "farm".

23 Claims, 12 Drawing figures

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L1: Entry 12 of 43 File: USPT Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870621 A
TITLE: Quadrilateral multichip computer systems and printed circuit boards therefor

Detailed Description Paragraph Table (61):

PIN I/O
BUFFER NAME NO. TYPE TYPE FUNCTION

PCI
System Terminals PCLK 163 I CMOS Bus Clock. Provides timing for all transactions on the PCI bus. RSTIN 164 I CMOS Reset. Forces the PCU to a known state. PCI Address and Data Terminals AD31 166 I/O CMOS/ Address/data bus. During the address AD30 167 I/O 12 mA phase of a PCI cycle, AD31-AD0 contain a AD29 168 I/O 32-bit address. During the data phase, AD28 169 I/O AD31-AD0 contain data. AD27 171 I/O AD26 172 I/O AD25 173 I/O AD24 174 I/O AD23 178 I/O AD22 179 I/O AD21 180 I/O AD20 181 I/O AD19 183 I/O AD18 184 I/O AD17 185 I/O AD16 186 I/O AD15 197 I/O AD14 198 I/O AD13 199 I/O AD12 200 I/O AD11 202 I/O AD10 203 I/O AD9 204 I/O AD8 205 I/O AD7 208 I/O AD6 1 I/O AD5 2 I/O AD4 3 I/O AD3 5 I/O AD2 6 I/O AD1 7 I/O AD0 8 I/O C/BE3 175 I CMOS Bus commands C and byte enables BE are C/BE2 187 I multiplexed on these PCI pins. During C/BE1 196 I the address phase, C/BE3-C/BE0 define C/BE0 207 I the bus command. During the data phase, C/BE3-C/BE0 are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C/BE0 applies to byte 0, and C/BE3 to byte 3. PAR 194 O 12 mA Parity. During the data phase of PCI reads; the chip calculates even parity across AD31 - 0 and C/BE3 - 0 and outputs the result on PAR. PCI Interface control Terminals FRAME 188 I CMOS Cycle frame. Driven by the current mas- ter to indicate the beginning and dura- tion of an access. FRAME is asserted to indicate that a bus transaction is be- ginning. While FRAME is asserted data transfers continue. When FRAME is deasserted the transaction is in the final data phase. TRDY 191 O 12 mA Target ready. Indicates the PCUs ability to complete the current data phase of the transaction. TRDY is used in con- junction with IRDY. A data phase is com- leted on any clock where both TRDY and IRDY are sampled asserted. During read, TRDY indicates that valid data is present on AD31-AD0. During a write, it indicates that the PCU is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. IRDY 189 I CMOS Initiator ready. Indicates the bus master's ability to complete the current data phase of the transaction. IRDY is used in conjunction with TRDY. A data phase is completed on any clock where both IRDY and TRDY are sampled asserted. During a write, IRDY indicates that val- id data is present on AD31-AD0. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. STOP 193 O 12 mA Stop. Indicates that the PCU is request- ing the PCI bus master to stop the current transaction. DEVSEL 192 O 12 mA Device select. When asserted, DEVSEL indicates that the PCU has decoded its address as the target of the current access. IDSEL 176 I CMOS Initiaiization device select. Selects the PCU during configuration accesses. This signal can be connected to one of the upper 24 PCI bus 104 address lines.

PIN NO.
SLOT SLOT I/O BUFFER NAME A.sup..theta. B.sup..theta. TYPE TYPE FUNCTION

PCMCIA
PC Card Interface Controller (Slots A and B) BVD1 126 63 I CMOS Battery voltage detect 3. Gener- (STSCHG) ated by memory PC cards that (RI) include batteries. This signal is used with BVD2 as an indication of the condition of the batteries on a memory PC card. Both BVD1 and BVD2 are kept high when the battery is good. When

h e b b cg b cc e

BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer servicable and the data in the memory PC card is lost. (Status change). This signal is used to alert the system to changes in the RDY/BSY, WP, or BVD conditions of the I/O PC card. (Ring indicate) This signal is used by modem cards to indicate ring detection. BVD2 125 62 I CMOS Battery voltage detect 2. Gener- (SPKR) ated by memory PC cards that include batteries. This signal is used with BVD1 as an indication of the condition of the batteries on a memory PC card. Both BVD1 and BVD2 are kept high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC card is lost. (Speaker). This binary audio signal is an optional signal available only when the card and socket have been configured for the I/O interface. The audio signals from card A and B can be combined by the PCU and output on terminal SPKROUT. CA25 110 48 O 2 mA Card address. Drives PC card CA24 108 46 O address lines. CA25 is the CA23 106 44 O most-significant bit. CA22 104 42 O CA21 102 40 O CA20 100 38 O CA19 98 36 O CA18 95 33 O CA17 93 31 O CA16 103 41 O CA15 105 43 O CA14 99 37 O CA13 96 34 O CA12 107 45 O CA11 90 28 O CA10 86 23 O CA9 92 30 O CA8 94 32 O CA7 109 47 O CA6 111 49 O CA5 113 51 O CA4 114 52 O CA3 115 53 O CA2 118 56 O CA1 119 57 O CA0 120 58 O *Terminal name is preceded with A.sub.--. As and example, the full name for terminal 126 is A.sub.-- BVD1. Terminal name is preceded with B.sub.--. As an example, the full name for terminal 63 is B.sub.-- BVD1. IORD 89 27 O 2 mA I/O read. This signal is driven low by the PCU to enable I/O PC card data output during host I/O read cycles. IOWR 91 29 O 2 mA I/O write. This signal is driven low by the PCU to strobe write data into I/O PC cards during host I/O write cycles. OE 88 25 O 2 mA Output enable. This output is driv- en low by the the PCU to enable memory PC card data output during host memory read cycles. REG 117 55 O 2 mA Attribute memory select. The REG signal remains high for all common memory accesses. When this signal is asserted, access is limited to attribute memory (OE or WE active) and to the I/O space (IORD or IOWR active). Attribute memory is a sep- arately accessed section of card memory and is generally used to re- cord card capacity and other con- figuration and attribute informa- tion. WE/PRGM 101 39 O 2 mA Write enable/program. This output signal is used for strobing memory write data into memory PC cards. This signal is also used for memory PC cards that employ programmable memory technologies. RDY/BSY 122 60 I CMOS Ready/busy. The ready/busy function (IREQ) is provided by the RDY/BSY signal when the PC card and the host sock- et are configured for the memory-only interface. This input is driven low by the memory PC cards to indicate that the memory card circuits are busy processing a previous write command. This signal is set high when memory PC cards are ready to accept a new data transfer command. (Interrupt request). This signal is asserted by an I/O PC card to indi- cate to the host that a device on the I/O PC card requires service by the host software. The signal is held at the inactive level when no interrupt is requested. RESET 112 50 O 2 mA PC card reset. Forces a hard reset to a PC card. WAIT 123 61 I CMOS Bus cycle wait. Driven by a PC card to delay completion of the memory or I/O cycle that is in progress. CIS3V 121 59 I CMOS Card is 3.3 volt. This signal indi- cates if the PC card can be powered at 3.3 volts. Cards that can oper- ate at 3.3 volts should assert CIS3V. Cards that require 5 volts do not supply an output signal to drive the CIS3V input; therefore an external pullup resistor is connected to CIS3V to prevent this output from floating. Terminal name is preceded with A.sub.--. As an example, the full name for

Detailed Description Paragraph Table (67):

Name	Access	Description	Bit
			7-5 --

R/W Reserved 4 GPICHG R GPI change. 0 = No change detected on GPI signal. 1= A change has been detected on GPI signal. 3 CDCHG R Card detect change. 0 = No change detected on either CD1 CD2 signals. 1 = A change has been detected on either CD1 or CD2 signals. 2 RDYCHG R Ready change. 0 = No low-to-high change detected on RDY/BSY. 1 = Detected low-to-high change of the RDY/BSY signal indicating that the memory PC card is ready to accept new data transfer. 1 BWARN R Battery warning. 0 =

h e b b cg b cc e

Battery-warning condition not detected 1 = Battery-warning condition detected 0 BDEAD R Battery dead. 0 = Battery-dead condition not detected 1 = Battery-dead condition detected

Address Window Enable Register. PCI Addresses (hex): Socket A:86 Offset (hex):Socket A:06 Socket B: C6 Socket B: 46 The address window enable register controls the enabling of the memory and I/O-mapping windows to the PC card memory or I/O space. I/O window enables control I/O accesses within the I/O address for the window specified. When PC card enables are generated, I/O accesses pass addresses from the system bus directly through to the PC Card

7 IW1EN R/W I/O-window 1 enable. 0 = Disable. 1 = Enable 6 IW0EN R/W I/O-window 0 enable. 0 = Disable 1 = Enable. 5 -- R/W Reserved 4 MW4EN R/W Memory-window 4 enable. 0 = Disable. 1 = Enable. 3 MW3EN R/W Memory-window 3 enable. 0 = Disable. 1 = Enable. 2 MW2EN R/W Memory-window 2 enable. 0 = Disable. 1 = Enable. 1 MW1EN R/W Memory-window 1 enable. 0 = Disable. 1 = Enable. 0 MW0EN R/W Memory-window 0 enable. 0 = Disable. 1 = Enable.

Global Control Register PCI Addresses (hex): Socket A: 9E Offset (hex):Socket A: 1E Socket B: DE Socket B: 5E

7-5 -- R/W Reserved 4 BIREQLM R/W Card B IREQ level mode interrupt enable. 0 = B.sub.-- IREQ is pulse mode. 1 = B.sub.-- IREQ is level mode 3 AIREQLM R/W Card A IREQ level mode interrupt enable. 0 = A.sub.-- IREQ is pulse mode. 1 = A IREQ is level mode 2 XWBCSC R/W Explicit write back of card status change interrupt acknowledge. 0 = CSC interrupts cleared by read of Card Status Change Register. 1 = SCS interrupts cleared by explicit write back of 1 to status flags in Card Status Change Register. 1 CSCLM R/W CSC level mode interrupt enable. 0 = CSC interrupts are pulse mode. 1 = CSC interrupts are level mode. 0 PWRDN R/W Chip power down. 0 = Normal operation. 1 = Power down enabled.

Card Detect and General Control Register CI Addresses (hex):Socket A: 96 Offset (hex):Socket A: 16 Socket B: D6 Socket B: 56

7-4 -- R/W Reserved 3 GPITRAN R/W GPI transition control. 0 = GPI high to low transition causes CSC interrupt. 1 = GPI low to high transition causes CSC interrupt. 2 GPIEN R/W GPI enable. 0 = CSC interrupts from GPI disabled. 1 = CSC interrupts from GPI enabled. 1 CONFRES R/W Configuration reset enable. 0 = Normal operation. 1 = Reset configuration registers for slot when CD1 and CD2 go high. 0 -- R/W Reserved.

Interrupt Registers Interrupt and General Control Register PCI Addresses (hex): Socket A:83 Offset (hex): Socket A:03 Socket B: C3 Socket B: 43 This read/write Interrupt and General Control register controls the interrupt steering for the PC card I/O interrupt as well as general control of the PCU

7 CRIEN R/W Ring indicate enable. The ring indicate enable bit has no function when the PC card type bit is set to 0 (memory PC card). For I/O PC cards: 0 = The STSCHG/RI signal from the I/O PC card is used as the STSCHG signal. The current status of the signal is then available to be read from the interface status register and this signal can be configured as a source for the card status change interrupt. 1 = The STSCHG/RI signal from the I/O PC card is used as a ring indicator signal and is passed through to the SMI output. 6 CRESET R/W PC card RESET. This is a software reset to the PC card. 0 = Drive card RESET active high. 1 = Drive card RESET active low. 5 CTYPE R/W PC card type (memory card or I/O card). 0 = Selects a memory PC card. 1 = Selects an I/O PC card and enables the PC card interface multiplexer for routing of PC card I/O signals. 4 SMIEN R/W SMI enable. 0 = CSC interrupts routed to one or of the IRQ lines according to bits 7-4 in the Card Status Change Configuration register 1 = CSC interrupts output on the SMI 3-0 CINT3-0 R/W This field selects the routing for PC card I/C interrupLs. CINT3 CINT2 CINT1 CINT0 Level 0 0 0 0 IRQ not selected 0 0 0 1 Reserved. 0 0 1 0 Reserved. 0 0 1 1 IRQ3 enabled 0

1 0 9 IRQ4 enabled 0 1 0 1 IRQ5 enabled 0 1 1 0 Reserved 0 1 1 1 IRQ7 enabled 1 0 0 0 Reserved 1 0 0 1 IRQ9 enabled 1 0 1 0 IRQ10 enabled 1 0 1 1 IRQ11 enabled 1 1 0 0 IRQ12 enabled 1 1 0 1 Reserved 1 1 1 0 IRQ14 enabled 1 1 1 1 IRQ15 enabled

Card Status Change Interrupt Configuration Register PCI Addresses (hex): Socket A: 85 Offset (hex):Socket A: 05 Socket B: C5 Socket B: 45 This register controls interrupt steering of the card status change interrupt and the card status change interrupt enables.

7-4 SINT3-0 R/W This field selects the routing for CSC interrupts. This field is ignored if bit SMIEN in the Interrupt and General Control register is set to 1. SINT3 S1NT2 SINT1 SINT0 Interrupt Request Level 0 0 0 0 IRQ not selected. 0 0 0 1 Reserved. 0 0 1 0 Reserved. 0 0 1 1 IRQ3 enabled. 0 1 0 0 IRQ4 enabled. 0 1 0 1 IRQ5 enabled. 0 1 1 0 Reserved. 0 1 1 1 IRQ7 enabled. 1 0 0 0 Reserved. 1 0 0 1 IRQ9 enabled. 1 0 1 0 IRQ10 enabled. 1 0 1 1 IRQ11 enabled. 1 1 0 0 IRQ12 enabled. 1 1 0 1 Reserved. 1 1 1 0 IRQ14 enabled. 1 1 1 1 IRQ15 enabled. 3 CDEN R/W Card detect enable. 0 = Disables the generation of a card change interrupt when the card detect signals change state. 1 = Enables a card status change interrupt when a change has been detected on the CD1 or CD2 signals. 2 RDYEN R/W Ready enable for memory PC cards. This bit is ignored when the interface is configured for I/O PC cards. 0 = Disables the generation of a card status change interrupt when a low-to-high transition has been detected on the RDY/BSY signal. 1 = Enables a card status change interrupt when a low-to-high transition has been detected on the RDY/BSY signal. 1 BWRNEN R/W Battery warning enable for memory PC cards. This bit is ignored when the interface is configured for I/O PC cards. 0 = Disables the generation of a card status change interrupt when a battery warning condition has been detected. 1 = Enables a card status change interrupt when a battery warning condition has been detected. 0 BDEADEN R/W Battery dead enable (STSCHC). 0 = Disables the generation of a card status change interrupt. This bit is ignored when the interface is configured for I/O PC cards and the CRIEN bit in the Interrupt and General Control register is set to 1. 1 = (For memory PC Cards) Enables a Card

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L1: Entry 12 of 43 File: USPT Feb 9, 1999

US-PAT-NO: 5870621
DOCUMENT-IDENTIFIER: US 5870621 A

TITLE: Quadrilateral multichip computer systems and printed circuit boards therefor

DATE-ISSUED: February 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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Chen; Edward	Panchiao City			TW
Edgeworth, III; Edwin P.	Mesquite	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
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APPL-NO: 08/ 363661 [PALM]
DATE FILED: December 22, 1994

INT-CL: [06] H05 K 1/00

US-CL-ISSUED: 395/820.32; 395/750.01, 257/499, 361/780, 364/491
US-CL-CURRENT: 712/32; 257/499, 361/780, 713/300

FIELD-OF-SEARCH: 395/800, 395/800.07, 395/800.32, 395/750.01, 364/488-491, 257/499, 361/780

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	4576664	March 1986	Bittorf et al.	364/131
☐	5122691	June 1992	Balakrishnaw	326/86
☐	5168024	December 1992	Smith et al.	395/375
☐	5264746	November 1993	Ohmae et al.	326/93
☐	5355453	October 1994	Row et al.	395/200.09

h e b b g e e e f c e e ge

☐ 5428499 June 1995 Szerlip et al. 361/328

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OPTi Pentium Brochure, Pentium Adaptive Write Back, 1992.
OPTi AT Brochure, Performance Upgrade Chipset for 486/Pentium Processors, 1993.
EFAR Microsystems, 386 Chip UP grade 486, SWIFT-IDE, Sep. 6, 1994.

ART-UNIT: 273

PRIMARY-EXAMINER: Bowler; Alyssa H.

ASSISTANT-EXAMINER: Fallausbee; John T.

ATTY-AGENT-FIRM: Burton; Dana L. Hollander; James F. Donaldson; Richard L.

ABSTRACT:

A computer system (6) includes a printed circuit board (302), a microprocessor chip (102), a peripheral unit chip (110), a card interface chip (112), and a display controller chip (114) mounted on the printed circuit board (302) at vertices of a quadrilateral (303). A clock buffer chip (180) is mounted on the printed circuit board (302) in the interior of the quadrilateral (303) and connected to each of the microprocessor chip (102), peripheral unit chip (110), card interface chip (112), and display controller chip (114). Other circuits, systems, and methods are disclosed.

21 Claims, 105 Drawing figures

L1: Entry 20 of 43 File: USPT Nov 24, 1998

DOCUMENT-IDENTIFIER: US 5841287 A
TITLE: System for detecting motherboard operation to ensure compatibility of a microprocessor to be coupled thereto

Detailed Description Text (2):
Turning now to the drawings, FIG. 1 illustrates a system 10 for determining operation of a printed circuit board (PCB). Preferably, PCB is a motherboard configured within the chassis of a personal computer. PCB 12 preferably comprises one or more dielectrically spaced layers, each of which comprise numerous printed conductors. Those conductors embody numerous signals, including a signal indicative of a system bus frequency (SYS CLK), a processor core voltage (VCC SN), a processor input/output voltage (VCC I/O), and clock multiplier signal voltage (BF0, BF1 and BF2). The signals of interest needed for detection by probe 14 can be contacted by a series of receptors 16 extending from probe 14. Receptors 16 align with and contact corresponding conductors within PCB 12. Preferably, receptors 16 align with terminal ends of the conductors, those terminal ends accumulated within, for example, a socket 18. Socket 18 occupies a relatively small portion of one surface of PCB 12. Socket 18 preferably comprises a plurality of mating receptors (not shown) arranged to electrically communicate with receptors 16 such that a plurality of electrical connections can be releasably made between probe 14 and socket 18. According to one embodiment, receptors 16 align with pins normally associated with a microprocessor, and that pins of interest within the microprocessor are substituted by corresponding receptors of probe 14. Thus, system clock, processor core and input/output voltages, ground, and clock multiplier pins extending from probe 14 match the arrangement at which those pins would normally extend from a microprocessor into socket 18.

First Hit Fwd Refs

☐ Generate Collection Print

L1: Entry 20 of 43 File: USPT Nov 24, 1998

US-PAT-NO: 5841287
DOCUMENT-IDENTIFIER: US 5841287 A

TITLE: System for detecting motherboard operation to ensure compatibility of a microprocessor to be coupled thereto

DATE-ISSUED: November 24, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Duley; Raymond S.	Buda	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 08/ 805178 [PALM]
DATE FILED: February 26, 1997

INT-CL: [06] G01 R 31/28, G06 F 3/00

US-CL-ISSUED: 324/537; 324/158.1, 324/538, 324/555, 395/500
US-CL-CURRENT: 324/537; 324/158.1, 324/538, 324/555

FIELD-OF-SEARCH: 324/537, 324/538, 324/555, 324/556, 324/73.1, 324/121R, 324/133, 324/158.1, 324/755, 324/763, 364/480, 364/481, 364/483, 364/484, 364/550, 364/551.01, 395/551, 395/555, 395/556, 395/653, 395/835, 395/836, 395/837, 395/838, 395/500, 702/57, 702/64, 702/75, 702/116, 702/117, 368/113, 368/118, 368/120

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4833397	May 1989	McMuray, Jr.	324/73.1
☐	4862067	August 1989	Brune et al.	324/73.1
☐	5546563	August 1996	Chuang	395/500
☐	5551012	August 1996	Chuang et al.	395/500

ART-UNIT: 288

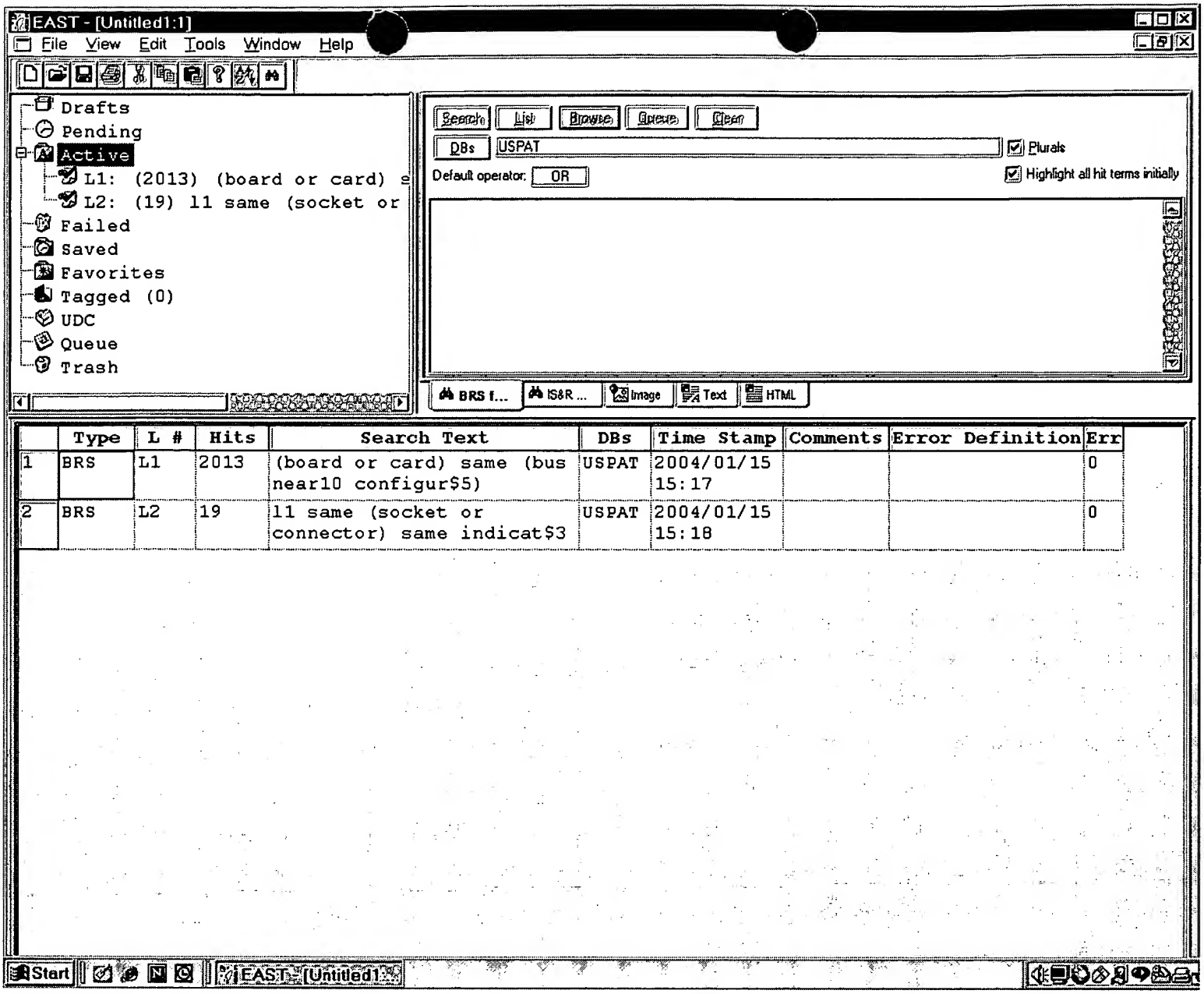
PRIMARY-EXAMINER: Do; Diep N.

ATTY-AGENT-FIRM: Kowert; Robert C. Conley, Rose & Tayon Daffer; Kevin L.

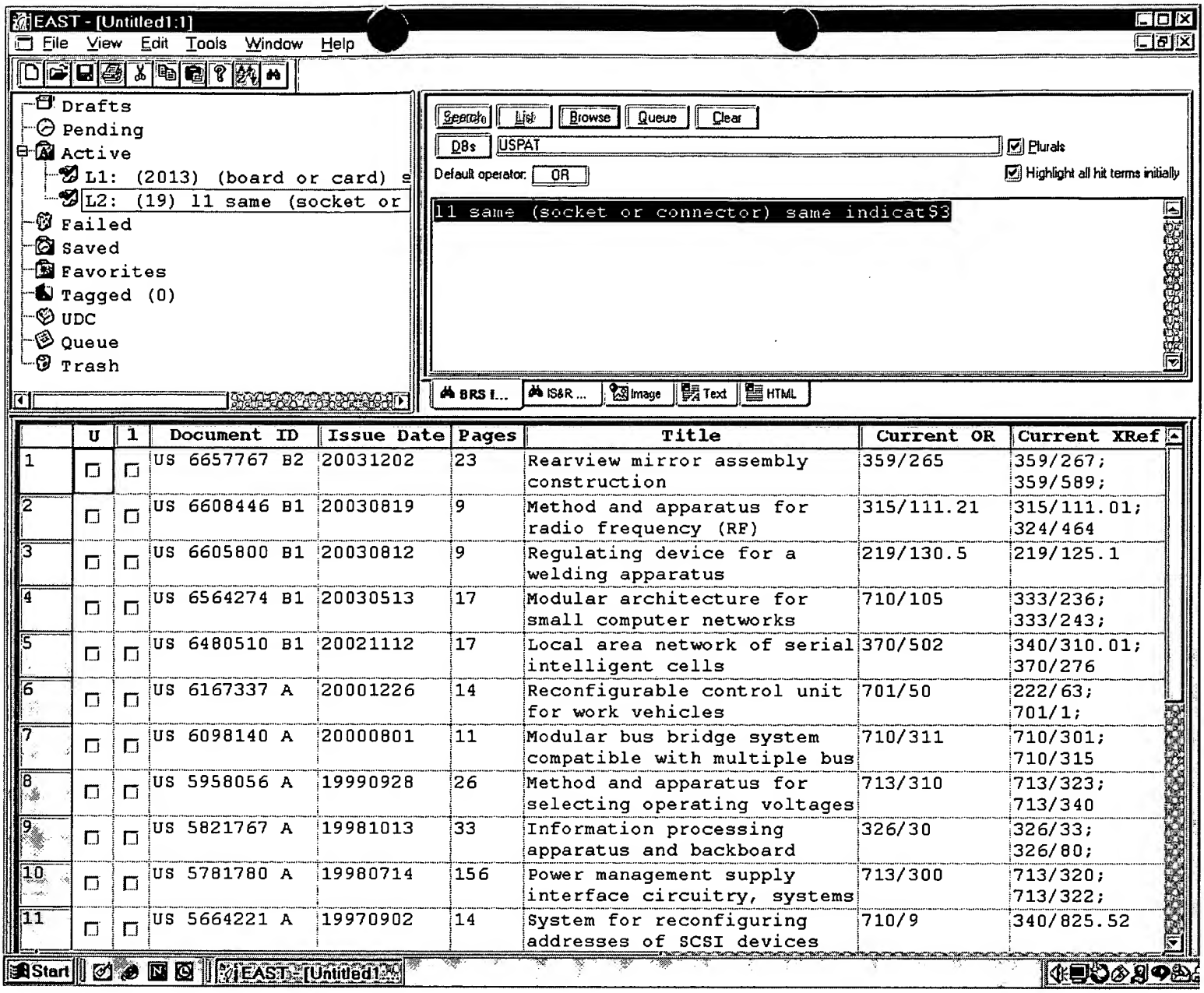
ABSTRACT:

One or more detection circuits are provided for determining the operation of a motherboard prior to placing a microprocessor upon that motherboard. The detection circuit determines a particular way in which the motherboard is configured by ascertaining, for example, a power supply voltage and a clocking frequency output from the motherboard. A probe is used, in combination with the detector circuits, to determine motherboard operation at a socket to which, for example, a microprocessor can be coupled. Jumpers or switches upon the motherboard can be readily found by activating a switch and looking for a response upon the detection circuit output. If a response is not found, the jumper or switch is returned, and another jumper or switch is activated. Once the jumper or switch used for changing system clock speed and/or processor voltage is located, then a display is read as to those parameters to ensure the parameters match the processor specification. Reading the motherboard configuration and/or reconfiguring the motherboard to a different operation parameter proves beneficial in ensuring its output compatibility to a microprocessor to be inserted upon the motherboard socket.

23 Claims, 7 Drawing figures



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	2013	(board or card) same (bus near10 configur$5)	USPAT	2004/01/15 15:17			0
2	BRS	L2	19	l1 same (socket or connector) same indicat$3	USPAT	2004/01/15 15:18			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6657767 B2	20031202	23	Rearview mirror assembly construction	359/265	359/267; 359/589;
2	☐	☐	US 6608446 B1	20030819	9	Method and apparatus for radio frequency (RF)	315/111.21	315/111.01; 324/464
3	☐	☐	US 6605800 B1	20030812	9	Regulating device for a welding apparatus	219/130.5	219/125.1
4	☐	☐	US 6564274 B1	20030513	17	Modular architecture for small computer networks	710/105	333/236; 333/243;
5	☐	☐	US 6480510 B1	20021112	17	Local area network of serial intelligent cells	370/502	340/310.01; 370/276
6	☐	☐	US 6167337 A	20001226	14	Reconfigurable control unit for work vehicles	701/50	222/63; 701/1;
7	☐	☐	US 6098140 A	20000801	11	Modular bus bridge system compatible with multiple bus	710/311	710/301; 710/315
8	☐	☐	US 5958056 A	19990928	26	Method and apparatus for selecting operating voltages	713/310	713/323; 713/340
9	☐	☐	US 5821767 A	19981013	33	Information processing apparatus and backboard	326/30	326/33; 326/80;
10	☐	☐	US 5781780 A	19980714	156	Power management supply interface circuitry, systems	713/300	713/320; 713/322;
11	☐	☐	US 5664221 A	19970902	14	System for reconfiguring addresses of SCSI devices	710/9	340/825.52

US-PAT-NO: 6098140

DOCUMENT-IDENTIFIER: US 6098140 A

TITLE: Modular bus bridge system compatible with multiple bus pin configurations

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Detailed Description Text - DETX (27):

FIG. 13 depicts the operation of the bus bridge 100 during the bus interface configuration process. This operation typically results when the bus bridge processor executes instructions stored in the bus bridge memory. When the process is started, the bus bridge scans the connectors and reads various hardware registers in step 1360. The scan could be a conventional PCI operation. The hardware registers are located on the various boards and contain ID bits that indicate the type of bus interface capability on the board.

US006098140A

United States Patent [19]

Pecone et al.

[11] Patent Number: 6,098,140

[45] Date of Patent: *Aug. 1, 2000

[54] **MODULAR BUS BRIDGE SYSTEM COMPATIBLE WITH MULTIPLE BUS PIN CONFIGURATIONS**

[75] Inventors: Victor Key Pecone, Lyons; Dwayne Howard Swanson, Westminster, both of Colo.

[73] Assignee: Adaptec, Inc., Milpitas, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 09/096,096

[22] Filed: Jun. 11, 1998

[51] Int. Cl.[7] G06F 13/00

[52] U.S. Cl. 710/129; 710/102

[58] Field of Search 710/100, 105, 710/129, 126, 102, 103; 711/113, 114, 118

[56] References Cited

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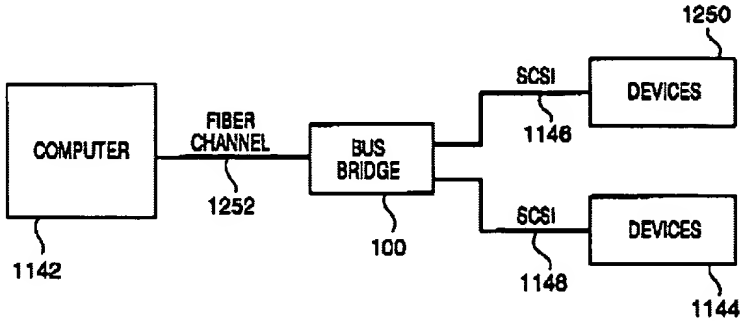
Primary Examiner—Glenn A. Auve

Attorney, Agent, or Firm—Duft, Graziano & Forest, P.C.

[57] **ABSTRACT**

The invention is a bus bridge for connecting a computer to peripheral devices over pluraliity of different bus interface configurations. The bus bridge comprises a motherboard and daughterboards. The daughterboards can be connected to the motherboard or to other daughterboards to create a new bus interface configuration. The bus bridge detects the new bus interface configuration and retrieves operating parameters to implement the new bus interface configuration. In some embodiments of the invention, the bus interface configuration is a fiber channel to the computer, a first small computer system interface to a first group of the peripheral devices, and a second small computer system interface to a second group of the peripheral devices.

18 Claims, 5 Drawing Sheets



US-PAT-NO: 5821767

DOCUMENT-IDENTIFIER: US 5821767 A

TITLE: Information processing apparatus and backboard having on backboard side matching resistors suited to modules connected thereto

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Brief Summary Text - BSTX (19):

FIG. 2 shows an example of the general bus wiring configuration in which a reference numeral 0 indicates a printed circuit board called "backboard" including connectors 41 to 44 on which modules 1 to 4 to be connected to the bus are mounted. The connectors 41 to 44 are mutually linked with to each other via a bus wiring 10 called "main line". The main line 10 ends with terminal resistors or terminators 200 and 201. Namely, each end of the line 10 is provided with matched termination. In each of the terminators Rtt 200 and 201, one end thereof is linked with a termination voltage source Vtt 300.

US005821767A

United States Patent [19]

Osaka et al.

[11] Patent Number: 5,821,767

[45] Date of Patent: Oct. 13, 1998

[54] **INFORMATION PROCESSING APPARATUS AND BACKBOARD HAVING ON BACKBOARD SIDE MATCHING RESISTORS SUITED TO MODULES CONNECTED THERETO**

[75] Inventors: Hideki Osaka, Hiratsuka; Yuichiro Seki, Yokohama; Shigemi Adachi, Seto, all of Japan

[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[21] Appl. No.: 633,309

[22] Filed: Apr. 15, 1996

[30] Foreign Application Priority Data

Apr. 17, 1995 [JP] Japan 7-090708

[51] Int. Cl.[6] H03K 17/16; H03K 19/0175

[52] U.S. Cl. 326/30; 326/86; 326/80; 326/33

[58] Field of Search 326/30, 33, 81, 326/80, 86; 327/404, 321; 361/782, 765

[56] References Cited

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5,534,801	7/1996	Wu et al.	326/81
5,627,481	5/1997	Takahama et al.	326/30

Primary Examiner—Edward P. Westin
Assistant Examiner—Richard Roseen
Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

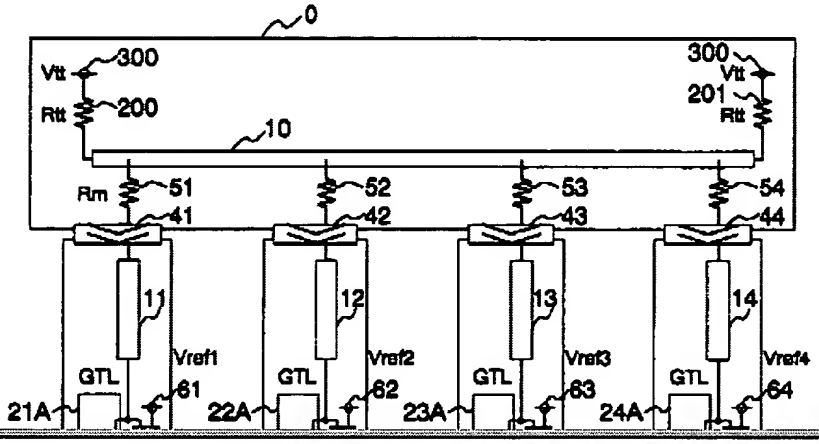
[57] ABSTRACT

In an information processing apparatus including a backboard having a bus for transmitting signals therethrough, at least one module, and a connector to connect the bus to the module, the backboard includes two terminators disposed respectively at both ends of the bus for providing matched termination according to a characteristic impedance of the bus to which the module is connected and a matching resistor disposed between the bus and the module. The matching resistor has a resistance value Rm represented as

$$Rm=Z1-k\cdot Z0/2(0.8<k<1.2)$$

where, Z1 indicates a characteristic impedance of the module, Z0 denotes the characteristic impedance of the bus, and k stands for a coefficient.

18 Claims, 20 Drawing Sheets



US-PAT-NO: 5664221

DOCUMENT-IDENTIFIER: US 5664221 A

TITLE: System for reconfiguring addresses of SCSI devices via a device address bus independent of the SCSI bus

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Detailed Description Text - DETX (7):

Referring to FIG. 2, a datacenter cabinet shelf enclosure 40 has eight device slots 42a, 42b, 42c, 42d, 42e, 42f, 42g, 42h, corresponding to slots 0 through 7, respectively. Slots 0 through 6 house SCSI I/O devices 26a-g (from FIG. 1). Typically, and as indicated in the figure, slot 7 is occupied by a power source (labeled "PS"), which supplies power to the shelf. Adjacent to slot 0 is the personality unit slot 44. As illustrated, the shelf enclosure 40 contains internally two independent SCSI buses, bus "A" 46 and bus "B" 48. Bus A 46 serves device slots 0, 2, 4 and 6, and bus B 48 serves device slots 1, 3 and 5. Personality unit back plane connector 50 routes the SCSI bus to and from the I/O devices. The manner in which the SCSI bus actually enters and exits the shelf enclosure will be more fully explained when FIG. 3 is discussed in detail. Still referring to FIG. 2, I/O device back plane connectors 52a, 52b, 52c, 52d, 52e, 52f, 52g corresponding to slots 0 through 6, respectively, receive the SCSI buses as shown and thus provide the interconnection between I/O device and SCSI bus. One or more of the device slots have a spare connector 54. In the example illustrated in the figure, slots 1 and 6 are provided with the spare connector 54 (shown in dashed lines) for receiving external termination or jumpered cards. Thus, the SCSI buses can be internally jumped to form one continuous bus that can be terminated internally within the personality unit or externally using a terminator card. In the configuration illustrated in FIG. 2, the spare connector at the slot 6 location contains a jumper board, thus joining bus A and bus B as one continuous bus. The bus automatically terminates in the personality unit 32, as will be discussed with reference to FIG. 3. Alternatively, the buses can be used as two, separate buses (dual bus configuration), each terminated internal to the shelf with a termination card. When the shelf is configured to contain two independent buses, duplicate device bus addresses can exist in the shelf, as long as they don't exist on the same bus. Further, duplicate device slot addresses can exist if only one of the slots to which the duplicate addresses are assigned is

US005664221A

United States Patent [19]

Amberg et al.

[11] Patent Number: 5,664,221

[45] Date of Patent: Sep. 2, 1997

[54] **SYSTEM FOR RECONFIGURING ADDRESSES OF SCSI DEVICES VIA A DEVICE ADDRESS BUS INDEPENDENT OF THE SCSI BUS**

[75] Inventors: **Mark F. Amberg**, Littleton; **William K. Miller**; **Frank M. Nemeth**, both of Colorado Springs; **Dwayne H. Swanson**, Westminster, all of Colo.

[73] Assignee: **Digital Equipment Corporation**, Maynard, Mass.

[21] Appl. No.: **557,473**

[22] Filed: **Nov. 14, 1995**

[51] Int. Cl.[6] G06F 13/10; G06F 9/00

[52] U.S. Cl. 395/829; 340/825.52

[58] Field of Search 395/829, 823, 395/287, 306, 200.2, 800, 281; 364/708.1; 340/825.52

[56] **References Cited**

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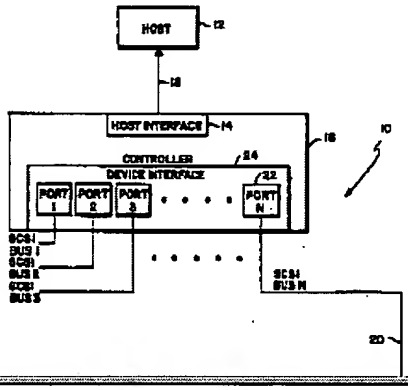
Primary Examiner—Gopal C. Ray

Attorney, Agent, or Firm—Ronald C. Hudgens; Cathy L. Peterson

[57] **ABSTRACT**

A system for assigning addresses to devices interconnected on a small computer system interface (SCSI) bus. A device address bus independent of the SCSI bus interconnects address assignable devices on the SCSI bus. The devices, each of which has a SCSI ID by which it is identified and being set with default bus address information representing the SCSI ID, are connected to one or more address lines on the device address bus. A system user can selectively reconfigure the bus addresses of the devices by utilizing a personality unit to override one or more bits of the bus address information. The personality unit includes a bus address selector, coupled to the device address bus, which selects address lines according to user input. The selecting of an address line effects a change in the default bus address information associated with the one or more devices connected to the selected address line.

3 Claims, 8 Drawing Sheets



US-PAT-NO: 4464120

DOCUMENT-IDENTIFIER: US 4464120 A

TITLE: Simulator systems for interactive simulation of complex dynamic systems

---------- KWIC ---------

Detailed Description Text - DETX (31):

The configuration of the local bus is such that short high bandwidth buses are provided between each of the neighbouring sockets i.e. a module which is placed in a given socket communicates with its neighbouring modules only on the electronic board 11. Consider for example a module which is placed in a socket e.g. the socket indicated at 40 in FIG. 2A. Due to the mentioned special local bus structure according to a first embodiment of the invention, the module in this socket 40 can only communicate with modules on the electronic board which are placed in neighbouring sockets occupying the positions N (indicated at 39), W (indicated at 38), S (indicated at 41) and E (indicated at 42). The configuration of the short buses is similar for all sockets in the electronic board so that for example two neighbouring modules always are connected in the same way independent of their positioning on the electronic board. The short buses carry analog and digital information signals between neighbouring modules.

United States Patent [19]

Jensen

[11] **Patent Number: 4,464,120**

[45] **Date of Patent: Aug. 7, 1984**

[54] **SIMULATOR SYSTEMS FOR INTERACTIVE SIMULATION OF COMPLEX DYNAMIC SYSTEMS**

[76] Inventor: **Kaj Jensen, 4, Kaarparken, DK-2800 Lyngby, Denmark**

[21] Appl. No.: **346,240**

[22] Filed: **Feb. 5, 1982**

[51] Int. Cl.³ G09B 9/00

[52] U.S. Cl. 434/219; 434/366; 434/224; 434/201; 364/801

[58] Field of Search 434/118, 219, 224, 365, 434/366, 201; 364/200, 801, 900, 419

[56] **References Cited**

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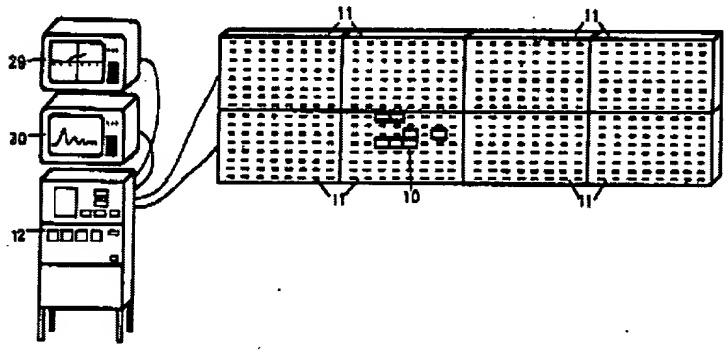
Primary Examiner—Richard C. Pinkham
Assistant Examiner—Leo P. Picard
Attorney, Agent, or Firm—Buckman and Archer

[57] **ABSTRACT**

A simulator and signal processing system for interactive simulation or signal processing of models of complex dynamic systems includes a range of basic hardware processor modules, each of which simulates or signal processes a system element corresponding e.g. to the symbols of System Dynamics. The hardware processor modules are placed in sockets arranged in regular rows and columns on an electronic planning board to form a flow diagram structure of the dynamic system to be simulated or signal processed. The electronic planning board comprises power lines for energizing the hardware processor modules and a high bandwidth local bus structure which transfer information signals between neighboring modules placed on the electronic planning board. The simulator and signal processing system permits a constant low simulation or signal processing time irrespective of the size or complexity of the model to be simulated or signal processed. The result of the simulation or signal processing is displayed on color monitors via the front-end system which performs as interface between the hardware processor modules on the electronic planning board and the monitors, or other peripherals.

2 Claims, 33 Drawing Figures



US-PAT-NO: 3891898

DOCUMENT-IDENTIFIER: US 3891898 A
See image for Certificate of Correction

TITLE: Panel board mounting and interconnection system for electronic logic circuitry

---------- KWIC ---------

Detailed Description Text - DETX (8):

FIG. 7 is a greatly enlarged sectional view of the three pins at the beginning of each of rows 23, 24 and 25 and it indicates the manner in which these pins make contact with the various conductive layers of panel board 11. The pins which are securely mounted in holes through board 11 may be electrically connected with different ones of the conductive layers. For example, pin 17A of row 24 is soldered as indicated by reference numeral 55 to conductive layer 14 (normally ground) and no contact is made with conductive layers 13 and 14. A space between the hole through board 11 and conductive planes 12 and 13 is shown in the drawing. End pin 17B of center row 25 makes contact with internal conductive plane 13 as indicated by solder filet 56. Pin 17C is shown as making no electrical contact to any of the conductive planes 12, 13 or 14 of the panel board. The basic purpose of most of the pins of the array is to provide interconnection between the integrated circuits 28 (FIG. 1) mounted in the socket ends of the pins, and other integrated circuits or external terminations by means of wrapped wires 33 and 34. If it is assumed that pin 17B is connected to center voltage plane 13, then the other pin in row 25 would normally be connected electrically to the ground plane 14. This would comport with the configuration of the printed circuit shown in FIG. 5 where bus 45 extends between the two pins 26, 27 of interior row 25. The three layer board shown in the drawing is particularly applicable to ECL circuitry because of speed of switching which creates noise and possible oscillation problems where wires are used to connect to internal third voltage sources such as bus bars or other printed circuit boards.

United States Patent [19]

[11] **3,891,898**

Damon

[45] **June 24, 1975**

[54] **PANEL BOARD MOUNTING AND INTERCONNECTION SYSTEM FOR ELECTRONIC LOGIC CIRCUITRY**

[75] Inventor: **Nail F. Damon, Cumberland, R.I.**

[73] Assignee: **Augat, Inc., Attleboro, Mass.**

[22] Filed: **Oct. 11, 1973**

[21] Appl. No.: **405,500**

[52] **U.S. Cl.** .. 317/101 CC; 174/DIG. 3; 339/17 CF
[51] **Int. Cl.** H05k 1/04
[58] **Field of Search** ..... 317/101 CC, 101 CM; 339/17 CF, 17 C, 147 R, 276 A; 174/DIG. 3; 29/203 MU, 203 P

[56] **References Cited**

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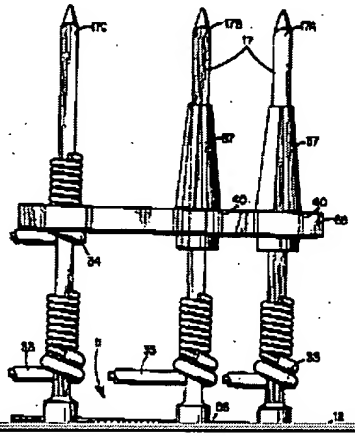
Primary Examiner—David Smith, Jr.
Attorney, Agent, or Firm—Weingarten, Maxham & Schurgin

[57] **ABSTRACT**

A panel board mounting and interconnection system for electronic logic circuitry. The system includes a panel board having arrays of wire wrapping pins projecting from one side, the other side of the board being adapted to receive integrated circuit modules and other electronic components for interconnection through leads connected to the wire wrapping pins. Selected pins within a single array are interconnected by means of a printed circuit substrate mounted to the pins parallel to the panel board, the printed circuit including passive elements such as resistors or capacitors or both.

8 Claims, 9 Drawing Figures



L3: Entry 8 of 28 File: USPT Mar 5, 2002

DOCUMENT-IDENTIFIER: US 6353870 B1
TITLE: Closed case removable expansion card having interconnect and adapter circuitry for both I/O and removable memory

Detailed Description Text (20):
FIG. 7 illustrates a PDA 200 equipped with a removable expansion card 100 having both I/O interconnect 140 and removable memory 120 in accordance with the present invention. The application specific circuitry of the expansion card may be used in conjunction with application specific software running on the PDA. This permits the application specific circuitry of the expansion card to make use of the output (e.g., display, sound) and input (e.g., tablet, buttons, any I/O ports) capabilities of the PDA for user interface functions associated with the specific application. In particular the PDA s display/input-tablet provides for virtual controls and visual indicators for the application. FIG. 8 illustrates some of the various types of I/O for which the PDA and removable expansion card of FIG. 7 may be equipped. Application-specific functions may include special-function mixed-signal electronics, special-function I/O, special-function data-pumps, and special-function accelerators.

Detailed Description Text (35):
The present invention permits a general purpose PDA to be customized as a portable/wearable personal environmental monitor. Equipped with the appropriate sensors and application-specific circuitry for sensor signal processing, such a device performs time-stamped data logging of environmental attributes such as ionizing radiation, temperature, and humidity. Similarly, a portable/wearable personal medial monitor data logs health-related attributes such as pulse, temperature, respiration, and blood pressure. The PDA s display/input-tablet provides the virtual controls and visual indicators for the monitoring devices.

US Reference Patent Number (13):
5611057

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☐ Generate Collection Print

L3: Entry 8 of 28 File: USPT Mar 5, 2002

US-PAT-NO: 6353870
DOCUMENT-IDENTIFIER: US 6353870 B1

TITLE: Closed case removable expansion card having interconnect and adapter circuitry for both I/O and removable memory

DATE-ISSUED: March 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Kevin J.	Palo Alto	CA		
Gifford; Micheal L.	San Leandro	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Socket Communications Inc.	Newark	CA			02

APPL-NO: 09/ 309373 [PALM]
DATE FILED: May 11, 1999

INT-CL: [07] G06 F 13/00, G06 F 1/16

US-CL-ISSUED: 710/301; 361/684, 361/686, 710/2, 711/115
US-CL-CURRENT: 710/301; 361/684, 361/686, 710/2, 711/115

FIELD-OF-SEARCH: 710/300-304, 710/2, 361/679-686

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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ART-UNIT: 2181

PRIMARY-EXAMINER: Lefkowitz; Sumati

ATTY-AGENT-FIRM: Smith; Bennett

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ABSTRACT:

Methods and apparatus for closed-case removable expansion cards having a removable memory enhance the utility of portable computer hosts, such as PDAs. In both a first and second embodiments the closed-case removable expansion cards preferably use a Type II CompactFlash form factor. In the first embodiment the removable memory is in combination with an external-I/O connector or attached external-I/O device, providing both I/O and memory functions in a single closed-case removable expansion card. This increases the expansion functional density for portable computer hosts, such as PDAs. That is, it increases the amount of functionality that can be accommodated within a given volume allocation for expansion devices. In the second embodiment the removable memory is a private memory for application specific circuitry within the closed-case-removable expansion card. This enhances the utility of portable computer hosts, such as PDAs, as universal chassises for application specific uses. The standard CompactFlash physical and electrical interface couples the application specific card to the host, which provides user interface functions for the application. The cards include a top located slot and an internal connector for accepting a MultiMediaCard as the private removable memory. In addition, the application specific card will generally have some manner of I/O to required external devices, such as scanning devices, sensors, or transducers. Otherwise, all functionality for the application specific function is self-contained within the application specific card.

40 Claims, 20 Drawing figures

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L4: Entry 1 of 1 File: USPT Aug 12, 1997

DOCUMENT-IDENTIFIER: US 5657455 A
TITLE: Status indicator for a host adapter

Brief Summary Text (9):
The data transfer circuit generates various signals that drive the status indicator circuit. The modules and configuration of the modules in the data transfer circuit are not essential aspects of this invention.

Brief Summary Text (12):
The status switching circuit prioritizes the coupling and decoupling of the output line to the various function input lines if more than one function enable line has an active signal. Specifically, in response to an active signal on the function disable line, the status switching circuit drives a signal on the status indicator terminal inactive, irrespective of the signals on the other function enable lines. Subsequently, in response to an inactive signal on the function disable line, the status switching circuit couples the output line to the first function input line that carries an active signal, if the first function enable line has an active signal. Hence the duration of the inactive signal on the status indicator terminal indicates the time needed to reset the host adapter integrated circuit.

Detailed Description Text (42):
After firmware is loaded successfully and a device identification number has been replaced as necessary, sequencer 314Q executes a write statement to address 1F, the address of status storage element 510A, to set input signals D5, D6 and D7 to 0, so that status storage element 510A drives signals FUNCTION1ENAB, FUNCTION1 inactive, e.g. low, and signal FUNCTION2ENAB- also inactive, e.g. high. In response, status switching circuit 520A supplies the inverse of signal DEVSCSIBSY on default function input line 523A as signal LED-. At this time, host adapter integrated circuit 214 is being configured and signal DEVSCSIBSY is inactive because host adapter integrated circuit 214 is not ready to support SCSI bus operations on the I/O bus.

Detailed Description Text (43):
From this point on, signal LED- goes active whenever host adapter integrated circuit 214 communicates with I/O bus 213 and goes inactive otherwise. Therefore, signal LED- provides a real time indication of the usage of I/O bus 213 by host adapter integrated circuit 214. As signal DEVSCSIBSY is generated inside host adapter integrated circuit 214, signal LED- remains inactive, thus independent of I/O Bus activity that is unrelated to the specific host adapter integrated circuit 214 that supplies signal DEVSCSIBSY.

Detailed Description Text (45):
Address 1F of status storage element 510A is within the address space of sequencer module 314Q in host adapter integrated circuit 214, and also within the address space of any device connected to system bus 250, such as microprocessor 211. To indicate that a predetermined path in software has been entered, the user merely inserts a statement to write to address 1F to configure signals D7, D6 and D5 of the write data bus included in internal bus 314B. Hence a program being executed by

either sequencer 314Q or by microprocessor 211 can be monitored for debugging or performance measurement by inserting statements to alternately write 1, 1, 0 and 1, 0, 0 on data lines D7, D6 and D5 respectively. This sequence of signals causes status indicator circuit 600A to supply the alternately active and inactive signal D6 as signal LED-.

Detailed Description Text (69):
In another embodiment, a pin RAMPS- of host adapter integrated circuit 214 can be used either as an input pin to indicate the presence of an external SRAM or as an output pin for a buffered clock signal PCLK. A circuit external to host adapter integrated circuit 214 uses the signal LED- that is generated in response to input signal IDDATCLK- to configure pin RAMPS- appropriately. If an external static RAM is present, pin RAMPS- is used as an input pin and must be grounded when PCI bus reset signal PCIRESET- is deasserted. Conversely, if the pin RAMPS- is to be used as an output pin for a buffered clock signal, for example, pin RAMPS- must be floated before the fourth clock cycle in signal IDDATCLK-.

Detailed Description Text (72):
Finally, if an external SRAM is present and it is desired to use pin RAMPS- as a buffered clock output pin, external circuity can use signal IDDATCLK- because signal IDDATCLK- is driven on line LED- by status indicator circuit 214I. Specifically, the external circuit grounds pin RAMPS- upon PCI bus reset and then uses signal LED- as a timer to float pin RAMPS- prior to fourth clock cycle in signal IDDATCLK-. Floating pin RAMPS- results in the internal circuitry sensing a high level on pin RAMPS-. Thus, if pin RAMPS- is low at reset and high at the fourth clock cycle, the internal circuit knows that an external SRAM is present, but pin RAMPS- can be used as an output pin for the buffered clock signal PCLK.

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End of Result Set

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L9: Entry 3 of 3 File: USPT Sep 24, 1996

DOCUMENT-IDENTIFIER: US 5559965 A

**** See image for Certificate of Correction ****

TITLE: Input/output adapter cards having a plug and play compliant mode and an assigned resources mode

Abstract Text (1):

An input/output adapter card for a standard bus in a computer system is disclosed that includes a nonvolatile memory that stores a plug and play identifier, a set of resource data, and a mode indication. The mode indication is programmed by an installation routine for the input/output adapter card to specify whether the input/output adapter card is plug and play compliant. The input/output adapter card accesses the mode indication and "plays" a configuration record from the nonvolatile memory to the configuration registers if the mode indication specifies that the computer system is not plug and play compliant. The configuration record mimics configuration writes to the configuration registers by a plug and play compliant computer system.

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First Hit Fwd Refs

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L9: Entry 3 of 3 File: USPT Sep 24, 1996

US-PAT-NO: 5559965
DOCUMENT-IDENTIFIER: US 5559965 A
**** See image for Certificate of Correction ****

TITLE: Input/output adapter cards having a plug and play compliant mode and an assigned resources mode

DATE-ISSUED: September 24, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Oztaskin; Ali S.	Beaverton	OR		
Allen; John L.	Hillsboro	OR		
Murthy; Ganesh	Hillsboro	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 299906 [PALM]
DATE FILED: September 1, 1994

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/284; 395/828, 395/830
US-CL-CURRENT: 710/104; 710/10, 710/8

FIELD-OF-SEARCH: 395/828, 395/829, 395/830, 395/831, 395/834, 395/284, 395/282, 395/700

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	5371892	December 1994	Petersen et al.	395/700
☐	5440693	August 1995	Arnold et al.	395/284
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ART-UNIT: 235

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

An input/output adapter card for a standard bus in a computer system is disclosed that includes a nonvolatile memory that stores a plug and play identifier, a set of resource data, and a mode indication. The mode indication is programmed by an installation routine for the input/output adapter card to specify whether the input/output adapter card is plug and play compliant. The input/output adapter card accesses the mode indication and "plays" a configuration record from the nonvolatile memory to the configuration registers if the mode indication specifies that the computer system is not plug and play compliant. The configuration record mimics configuration writes to the configuration registers by a plug and play compliant computer system.

26 Claims, 9 Drawing figures

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End of Result Set

Generate Collection Print

L1: Entry 1 of 1 File: USPT Mar 11, 1997

DOCUMENT-IDENTIFIER: US 5611057 A
TITLE: Computer system modular add-in daughter card for an adapter card which also functions as an independent add-in card

Detailed Description Text (8):
Although not explicitly shown in FIGS. 1A and 1B, various elements comprised on the daughter card 24 are interconnected to perform various SCSI operations, as is well known in the art. For example, the SCSI daughter card 24 preferably includes one or more SCSI controllers and corresponding SCSI connectors as well as associated termination logic. The daughter card 24 also may include SIMM sockets which receive corresponding memory modules, a processor or CPU which performs operations necessary to implement one or more RAID configurations as well as for controlling operations of the daughter card 24, a PCI interface chip, a plurality of LEDs for displaying the status of the card and optionally a bracket including an external SCSI connector. Thus the daughter card 24 comprises a fully functional PCI SCSI card and also functions as a daughter card to host SCSI adapter card 22.

Detailed Description Text (12):
Although not explicitly shown in FIGS. 2A and 2B, various elements comprised on the adapter card 22 are interconnected to perform various SCSI operations, as is well known in the art. For example, the SCSI adapter card 22 preferably includes a SCSI controller and a corresponding SCSI connector, associated termination logic, SIMM sockets which receive corresponding memory modules, and a processor or CPU which performs operations necessary to implement one or more RAID configurations as well as for controlling operations of the adapter card 22. The adapter card 22 also preferably includes a PCI interface chip, a plurality of LEDs for displaying the status of the card and an bracket 81 including an external SCSI connector 80. Thus the adapter card 22 comprises a fully functional PCI SCSI card.

Detailed Description Text (13):
The SCSI adapter card 22 includes two daughter card connectors 72 and 74 for receiving the optional add-in daughter card 24. In one embodiment, signal lines from the SCSI controller(s) on the adapter card 22 connect to pins on the daughter card connectors 72 and 74 to provide signals to the daughter card 24 when the daughter card 24 is mounted to the adapter card 22. In this embodiment, the CPU on the adapter card 22 preferably stores one or more bits indicating whether the daughter card 24 is connected as well as bits indicating whether SCSI controllers are included on the daughter card 24, whether internal SCSI channels are routed eternally, and whether SCSI devices are connected to the daughter card 24. For more information on the SCSI adapter 22 of the preferred embodiment, please see related copending application Ser. No. 08/351,848 referenced above.

Detailed Description Text (39):
When the daughter card 24 is mounted to the adapter card 22, the daughter card 24 preferably provides signals to the CPU 60 on the adapter card 22 indicating that the daughter card 24 is connected, how many SCSI controllers and corresponding SCSI channels are provided by the daughter card 24, and whether any respective internal SCSI channels are rerouted externally. The daughter card 24 also indicates whether

a SCSI cable and accompanying devices are connected to ports on the daughter card 24.

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L1: Entry 1 of 3 File: USPT Aug 12, 1997

US-PAT-NO: 5657455
DOCUMENT-IDENTIFIER: US 5657455 A

TITLE: Status indicator for a host adapter

DATE-ISSUED: August 12, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gates; Stillman F.	Los Gatos	CA		
Fannin; Charles S.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Adaptec, Inc.	Milpitas	CA			02

APPL-NO: 08/ 301458 [PALM]
DATE FILED: September 7, 1994

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/280; 395/284, 395/309, 395/312
US-CL-CURRENT: 710/100; 710/104, 710/316

FIELD-OF-SEARCH: 395/280, 395/284, 395/307, 395/309, 395/312

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4038644	July 1977	Duke et al.	364/900
☐	4419756	December 1983	Cheng-Quispe et al.	375/7
☐	4564794	January 1986	Kilen et al.	318/314
☐	4878166	October 1989	Johnson et al.	364/200

OTHER PUBLICATIONS

Data Book, Preliminary, AIC-7870 PCI Bus Master Single-Chip SCSI Host Adapter, Adaptec, pps. 1-1 through 1-8, 2-1 through 2-31, 8-1 through 8-11, Dec., 1993.
Data Book, Preliminary, AIC-7850 PCI Bus Master Single-Chip SCSI Host Adapter,

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Adaptec, pps. 1-1 through 1-6, 2-1 through 2-23, 8-1 through 8-11, Feb., 1994.

ART-UNIT: 235

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Travis; John

ATTY-AGENT-FIRM: Skjerven, Morrill, MacPherson, Franklin & Friel Gunnison; Forrest E. Suryadevara; Omkar K.

ABSTRACT:

A host adapter for transferring data between a system bus and an input/output (I/O) bus is implemented as an integrated circuit having a data transfer circuit and a status indicator circuit. The status indicator circuit selectively supplies one of a number of status signals from the data transfer circuit as a signal on a status indicator terminal of the host adapter. Therefore, a light emitting diode connected to the status indicator terminal indicates in real time the status of data transfer, such as usage of the system bus, or I/O bus, or execution time of one or more instructions by the host adapter.

34 Claims, 15 Drawing figures

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L1: Entry 2 of 3 File: USPT Mar 11, 1997

US-PAT-NO: 5611057
DOCUMENT-IDENTIFIER: US 5611057 A

TITLE: Computer system modular add-in daughter card for an adapter card which also functions as an independent add-in card

DATE-ISSUED: March 11, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pecone; Victor K.	Austin	TX		
Smith; Russell C.	Pflugerville	TX		
Lory; Jay R.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dell USA, L.P.	Austin	TX			02

APPL-NO: 08/ 376312 [PALM]
DATE FILED: January 20, 1995

PARENT-CASE:
CROSS-REFERENCES TO RELATED APPLICATIONS This is a continuation-in-part of copending application Ser. No. 08/351,848 titled "Computer System SCSI Adapter Card Including an Add-in Daughter Board Providing an External SCSI Connector For Modular and Upgradable SCSI Bus Routing Options" and filed Dec. 8, 1994, whose inventors are Victor Pecone and Jay Lory, and which is assigned to Dell USA, L.P. This is also a continuation-in-part of copending application Ser. No. 08/319,207 titled "PCI/PCI Bus Interface Controller with Non-coupled Peripheral Slave Bus Extension" and filed Oct. 6, 1994, whose inventors are Victor Pecone and Jay Lory, and which is assigned to Dell USA, L.P.

INT-CL: [06] H01 R 23/00

US-CL-ISSUED: 395/282; 361/784, 439/74
US-CL-CURRENT: 710/301; 361/784, 439/74

FIELD-OF-SEARCH: 361/784, 361/785, 439/74, 439/75, 395/281-282

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5099394	March 1992	Hood et al.	361/785
☐	5163219	November 1992	Akulow et al.	361/785
☐	5308248	May 1994	Davidge et al.	439/59
☐	5446869	August 1995	Padgett et al.	395/500
☐	5471590	November 1995	Melo et al.	395/288

ART-UNIT: 235

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Lefkowitz; Sumati

ATTY-AGENT-FIRM: Garrana; Henry N. Kahler; Mark P. Roberts; Diana L.

ABSTRACT:

A daughter card for mounting to an adapter card, wherein the daughter card includes adapter card connectors for mounting to the adapter card and also an edge connector for insertion directly into a computer slot so that the daughter card may also function as a stand-alone card. The daughter card is both mechanically and electrically compliant as an independent PCI add-in card and includes a PCI edge connector for insertion directly into a PCI slot. This provides additional modularity since the daughter card can be purchased and configured as a separate and independent PCI adapter card as well as for mating to a host adapter card to provide extra functionality to the host adapter card. In addition, since the daughter card can be directly inserted into the PCI bus, the daughter card provides greater component access and probing for testing. Further, the daughter card can be tested independently of the host adapter card during manufacturing functional test, thus providing more reliable testing.

21 Claims, 10 Drawing figures

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L1: Entry 3 of 3 File: USPT Jun 24, 1975

US-PAT-NO: 3891898
DOCUMENT-IDENTIFIER: US 3891898 A
**** See image for Certificate of Correction ****

TITLE: Panel board mounting and interconnection system for electronic logic circuitry

DATE-ISSUED: June 24, 1975

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Damon; Neil F.	Cumberland	RI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Augat, Inc.	Attleboro	MA			02

APPL-NO: 05/ 405500 [PALM]
DATE FILED: October 11, 1973

INT-CL: [] H05k 1/04

US-CL-ISSUED: 317/101CC; 174/DIG.3, 339/17CF
US-CL-CURRENT: 361/774; 361/792, 439/70, 439/75

FIELD-OF-SEARCH: 317/11CC, 317/11CM, 339/17CF, 339/17C, 339/147R, 339/276A, 174/DIG.3, 29/23MU, 29/23P

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3088087	April 1963	Colten	339/276A
☐	3197766	July 1965	Stein et al.	317/101D
☐	3325766	June 1967	Kolb et al.	339/17CF
☐	3740697	June 1973	Vanson	339/276A

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ART-UNIT: 217

PRIMARY-EXAMINER: Smith, Jr.; David

ATTY-AGENT-FIRM: Weingarten, Maxham & Schurgin

ABSTRACT:

A panel board mounting and interconnection system for electronic logic circuitry. The system includes a panel board having arrays of wire wrapping pins projecting from one side, the other side of the board being adapted to receive integrated circuit modules and other electronic components for interconnection through leads connected to the wire wrapping pins. Selected pins within a single array are interconnected by means of a printed circuit substrate mounted to the pins parallel to the panel board, the printed circuit including passive elements such as resistors or capacitors or both.

8 Claims, 9 Drawing figures

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